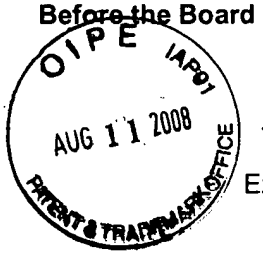
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Before the Board of Patent Appeals and Interferences



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In re Patent Application of
FLYNN
Serial No. 10/715,368
Filed: November 19, 2003
Title: DATA PROCESSING PERFORMANCE CONTROL

Atty Dkt. SCS-550-489
C# M#
Confirmation No. 9185
TC/A.U.: 2116
Examiner: M. Brown
Date: August 11, 2008

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

☐ **Correspondence Address Indication Form Attached.**

☐ **NOTICE OF APPEAL**
Applicant hereby **appeals** to the Board of Patent Appeals and Interferences from the last decision of the Examiner twice/finally rejecting applicant's claim(s). $510.00 (1401)/$255.00 (2401) $

☒ An appeal **BRIEF** is attached in the pending appeal of the above-identified application $510.00 (1402)/$255.00 (2402) $ 510.00

☐ Credit for fees paid in prior appeal without decision on merits -$ ( )

☐ A reply brief is attached. **(no fee)**

☐ Petition is hereby made to extend the current due date so as to cover the filing date of this paper and attachment(s)
One Month Extension $120.00 (1251)/$60.00 (2251)
Two Month Extensions $460.00 (1252)/$230.00 (2252)
Three Month Extensions $1050.00 (1253/$525.00 (2253)
Four Month Extensions $1640.00 (1254/$820.00 (2254) $

☐ "Small entity" statement attached.

Less month extension previously paid on -$( )

TOTAL FEE ENCLOSED $ 510.00

☒ **CREDIT CARD PAYMENT FORM ATTACHED.**

Any future submission requiring an extension of time is hereby stated to include a petition for such time extension. The Commissioner is hereby authorized to charge any deficiency, or credit any overpayment, in the fee(s) filed, or asserted to be filed, or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to our **Account No. 14-1140.** A duplicate copy of this sheet is attached.

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By Atty: Stanley C. Spooner, Reg. No. 27,393

Signature:

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Patent Application of
FLYNN
Serial No. 10/715,368
Filed: November 19, 2003

Confirmation No.: 9185
Atty. Ref.: 550-489
Group: 2116
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For: DATA PROCESSING PERFORMANCE CONTROL

* *

APPEAL BRIEF

On Appeal From Group Art Unit 2116

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Patent Application of

FLYNN — Atty. Ref.: 550-489

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* *

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APPEAL BRIEF

Sir:

I. REAL PARTY IN INTEREST

The real party in interest in the above-identified appeal is ARM Limited by virtue of an assignment of rights from the inventor to ARM Limited recorded November 19, 2003 at Reel 14716, Frame 852.

II. RELATED APPEALS AND INTERFERENCES

There are believed to be no related appeals, interferences or judicial proceedings with respect to the present application, other than the two Pre-Appeal

Brief Request for Review previously filed in this appeal on November 26, 2007 and on June 13, 2008.

III. STATUS OF CLAIMS

Claims 1-11 stand rejected under 35 USC §103 in the outstanding 5th and non-final Official Action mailed March 13, 2008 in view of Cooper (U.S. Patent 6,823,516) combined with Tobias (U.S. Patent 7,254,721). The above rejections of claims 1-11 are appealed.

IV. STATUS OF AMENDMENTS

No further response has been submitted with respect to the previous Final Official Action in this application other than the filing of the first Pre-Appeal Brief Request for Review which Panel decision was to reopen prosecution and was mailed December 20, 2007 (paper no. 20071217) and with respect to the fifth and non-final Official Action a second Pre-Appeal Brief Request for Review which Panel decision was to go to Appeal and was mailed July 3, 2008 (paper no. 20080702).

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

Appellant's specification and figures provide an explanation of the claimed invention set out in independent claims 1, 6 and 11, with each claimed structure and method step addressed as to its location in the specification and in the figures.

"1. Apparatus for processing data [generally shown in Figures 1 and 6 and discussed on page 6, line 12 to page 7, line 9 and page 12, lines 14-20 and elsewhere in the specification], said apparatus comprising:

a processor [the processor referenced to generally on page 6 is shown as processor 46 in Figure 6 (see specification at page 12, lines 15-16 confirming like elements in Figures 1 and 6) and discussed both on page 6, line 12 to page 7, line 9 and page 12, lines 14-20 and elsewhere in the specification] operable to perform data processing operations, said processor being operable to generate a performance control signal indicative of a desired data processing performance level of said processor [as discussed on page 6, line 19-22 and elsewhere in the specification]; and

at least one further circuit [elements 2, 4, 6 in Figures 1 and 6 and discussed on page 6, line 19 to page 7, line 2 and elsewhere in the specification], responsive to said performance control signal, to support said desired data processing performance level of said processor; wherein while responding to a change in performance control signal corresponding to a change from a first desired data processing performance level to a second desired data processing performance level, said at least one further circuit supports data processing of said processor at at least one intermediate data processing performance level [as shown in Figures 4 & 5 and discussed on page 9, line 27 to page 10, line 12, page 11, line 27 to page

12, line 12 and elsewhere in the specification] and said processor temporarily operates at said at least one intermediate data processing performance level during said change [as discussed on page 3, lines 21-30 and elsewhere in the specification]."

"6. A method of processing data, said method comprising the steps of:

performing data processing operations with a processor [the processor referenced to generally on page 6 is shown as processor 46 in Figure 6 (see specification at page 12, lines 15-16 confirming like elements in Figures 1 and 6) and discussed both on page 6, line 12 to page 7, line 9 and page 12, lines 14-20 and elsewhere in the specification], said processor being operable to generate a performance control signal indicative of a desired data processing performance level of said processor [as discussed on page 6, line 19-22 and elsewhere in the specification]; and

in response to said performance control signal, operating one or more further circuits so as to support said desired data processing performance level of said processor [elements 2, 4, 6 in Figures 1 and 6 and discussed on page 6, line 19 to page 7, line 2 and elsewhere in the specification]; wherein while responding to a change in performance control signal corresponding to a change from a first desired data processing performance level to a second desired data processing performance level, said operating step includes supporting data processing of said

processor at at least one intermediate data processing performance level [as shown in Figures 4 & 5 and discussed on page 9, line 27 to page 10, line 12, page 11, line 27 to page 12, line 12 and elsewhere in the specification] and said processor temporarily operates at said at least one intermediate data processing performance level during said change [as discussed on page 3, lines 21-30 and elsewhere in the specification]."

"11. Apparatus for processing data [shown generally in Figure 6 and elsewhere in the specification], said apparatus comprising:

a processor operable to perform data processing operations [the processor referenced to generally in conjunction with Figure 1 on page 6 is shown as processor 46 in Figure 6 (see specification at page 12, lines 15-16 confirming like elements in Figures 1 and 6) and discussed both on page 6, line 12 to page 7, line 9 and page 12, lines 14-20 and elsewhere in the specification], said processor being operable to generate a performance control signal indicative of a desired data processing performance level of said processor [as discussed on page 6, line 19-22 and elsewhere in the specification]; and

at least one further circuit, responsive to said performance control signal, for supporting said desired data processing performance level of said processor [elements 2, 4, 6 in Figures 1 and 6 and discussed on page 6, line 19 to page 7, line 2 and elsewhere in the specification]; wherein while responding to a change in

performance control signal corresponding to a change from a first desired data processing performance level to a second desired data processing performance level, said at least one further circuit comprising a means for supporting data processing of said processor at at least one intermediate data processing performance level [as shown in Figures 4 & 5 and discussed on page 9, line 27 to page 10, line 12, page 11, line 27 to page 12, line 12 and elsewhere in the specification] and said processor temporarily operates at said at least one intermediate data processing performance level during said change [as discussed on page 3, lines 21-30 and elsewhere in the specification]."

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-11 stand rejected under 35 USC §103 as being unpatentable over Cooper (U.S. Patent 6,823,516) in view of Tobias (U.S. Patent 7,254,721).

VII. ARGUMENT

Appellant's arguments include the fact that the burden is on the Examiner to first and foremost properly construe the language of the claims to determine what structure and/or method steps are covered by that claim. After proper construction of the claim language, the burden is also on the Examiner to demonstrate where a single reference (in the case of anticipation) or a plurality of

references (in the case of an obviousness rejection) teaches each of the structures and/or method steps recited in independent claims 1, 6 and 11.

Furthermore, the Court of Appeals for the Federal Circuit has stated in the case of *In re Rouffet*, 47 USPQ2d 1453, 1458 (Fed. Cir. 1998)

> to prevent the use of hindsight based on the invention to defeat patentability of the invention, this court **requires** the examiner to show a **motivation** to combine the references that create the case of obviousness. In other words, the Examiner **must show reasons** that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed. (Emphasis added).

In its recent decision, the U.S. Supreme Court in *KSR International Co. v. Teleflex Inc.*, 82 USPQ2d 1385 (April 2007), held that it is often necessary for a court to look to interrelated teachings of multiple patents, the effects of demands known to the design community or present in the marketplace and the background knowledge possessed by a person of ordinary skill in the art in order to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue. The Supreme Court held that "[t]o facilitate review, this analysis should be made explicit." *Id.* at 1396.

The Supreme Court in its *KSR* decision went on to say that it followed the Court of Appeals for the Federal Circuit's advice that "rejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be

some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness" (the Supreme Court quoting from the Court of Appeals for the Federal Circuit in *In re Kahn*, 78 USPQ2d 1329 (Fed. Cir. 2006)).

A. The Examiner previously ignored the limitations of independent claims 1, 6 and 11

Each of independent claims 1, 6 and 11 specifies that the "at least one further circuit" has an interrelationship with the processor so as to support "data processing of said processor at **at least one intermediate data processing performance level . . . during said change**" (emphasis added).

In the 5th and non-final rejection, page 3, section 3, the Examiner finally admits that the Cooper reference fails to disclose the claimed "at least one further circuit." The Examiner has now expanded this admission (over that previously made) to include a significant portion of each of the independent claims, i.e., "supports data processing of said processor at at least one intermediate data processing performance level during said change" [which is the change from the first desired data processing performance level to the second desired data processing performance level].

The Examiner now cites Tobias (USP 7,254,721) (instead of the previously cited Kobaysahi (USP 6,148,415)) as teaching "data processing of said processor at at least one intermediate data processing performance level . . . during said change."

As will be seen, Tobias also fails to contain any such teaching and that, combined with the fact that both Cooper and Tobias actually teaches "quiescence" between performance states, teaches away from any such disclosure and obviates the Examiner's rejections.

B. The Examiner misunderstands the Tobias reference teaching

In the paragraph bridging pages 3 and 4 of the 5th and non-final Official Action, the Examiner alleges that Tobias teaches that "said processor temporarily operates at said at least one intermediate data processing performance level during said change" and cites Tobias at column 4, line 64 to column 5, line 31. Both the conclusion and the reference are inaccurate and incorrect.

The cited portion of Tobias actually states:

> "the power management selects the maximum performance state P5 as the next performance state. Thus, if the performance state is always taken straight to the maximum performance state when a performance increase is required . . . there is less of a chance that a user could notice any performance degradation." (Column 5, lines 19-27). Similarly, "if a lower performance state is required, a next lower performance state is selected." (Column 5, lines 32-33).

Thus, Tobias clearly teaches that one sequentially steps from P1 to P2 to P3 to P4 to P5 when increasing processor speed and proceeds similarly when decreasing processor speeds. This is accomplished in Tobias because performance level is selected by controlling a programmable voltage ID (VID) field or core clock frequency control field (see the discussion at column 11, lines 54-58).

Most importantly, Tobias, when changing performance levels, issues a "stop grant" signal to indicate to the CPU core that the CPU core should stop execution of operating system and application code and **enter a stop grant state** (Tobias, column 11, line 54 through column 12, line 3). During the "stop grant state," **no processing takes place** and a new VID value is sent to a voltage regulator and the new clock frequency control value is supplied to the clock generation circuit (Tobias, column 13, lines 63-66). In Tobias, **only** after the new clock frequency and the new voltage have been stabilized, then the stop signal is deasserted and the CPU core resumes executing code (Tobias, column 14, lines 1-8).

Thus, in view of the above, Tobias clearly requires that the CPU **not operate** during performance level changes since it implements the "stop grant state." Thus, Tobias, like Cooper's "quiescent" state, requires a "stop grant state" in which the CPU does not operate "during said change" in data processing performance level.

As a result, neither Cooper nor Tobias teach the recited feature of Appellant's independent claims, i.e., the claimed "at least one further circuit" which supports data processing at **an intermediate data processing performance level** "during said change."

C. The Examiner errs in failing to identify any "reason" or "motivation" for combining Cooper and Tobias

In the partial paragraph at the top of page 4 of the 5th Official Action, the Examiner alleges that it would have been obvious to "add Tobias' power management control logic 507 to Cooper's system for adjusting CPU performance." As noted above, this would only substitute the Tobias "stop grant state" for the Cooper "quiescent" state and has nothing to do with the present independent claim limitation of supporting the processor "at said at least one intermediate data processing performance level during said change."

The Examiner suggests that the motivation "to do so would be to reduce the chance that any degradation is detected by a system user" and cites Tobias column 5, lines 40-41. However, the motivation discussed at the cited portion of Tobias is with respect to the stepwise changing of performance level from step P5 to P4 then to P3 then to P2, etc. It is this stepwise performance change that Tobias uses to "reduce the chance that any degradation is detected by a system user." These stepwise changes occur only during the "stop grant state" and thus, during the Tobias change, **there is no processor performance which could be degraded.**

The Examiner does not identify any teaching in either Cooper or Tobias which suggests processor operation at any intermediate data processing level **"during said change,"** (claims 1, 6 and 11, emphasis added) i.e., from P2 to P3 or vice versa.

Given that the Examiner will not and can not identify any disclosure of the operation "during said change," he certainly can't provide any rationale for picking and choosing elements from the Cooper and Tobias references and then combining them in the manner of Applicant's independent claim 1, i.e., in a manner such that "said processor temporarily operates at said at least one intermediate data processing performance level during said change."

In accordance with the recent Supreme Court decision in *KSR v. Teleflex,* it is incumbent upon the Examiner to articulate some "reason" for picking and choosing elements from the various prior art references and then combining them in the manner of the claimed invention. The Supreme Court specifically indicated that the examiner's rationale must be made explicit ("to facilitate review, this analysis should be made explicit." *KSR International Co. v. Teleflex, Inc.* 82 USPQ2d 1385, 1396 (SCT 2007)).

Because the Examiner has failed to provide any reason for combining the Cooper and Tobias references, he has failed to establish a *prima facie* case of obviousness under 35 USC §103 with respect to independent claims 1, 6 and 11.

D. The Examiner appears to ignore the fact that both Cooper and Tobias teach away from Appellant's claimed combination

As noted above, the Cooper reference clearly teaches away from Applicant's claimed "intermediate data processing level during said change" by

teaching that the processor is stopped in a "relatively quiescent state" during any such change. Tobias similarly requires, when changing power levels, the processor is stopped in the "stop grant state," i.e., the processor completes the last instructions and then stops.

Both the Cooper and Tobias references, in teaching no processor performance "during said change," would lead one of ordinary skill in the art away from the claimed invention of "at least one intermediate data processing performance level during said change." (independent claims 1, 6 & 11).

The fact that both cited references would lead one of ordinary skill in the art away from the claimed invention which continues to operate the processor at an intermediate performance level "during said change" is evidence which clearly rebuts any *prima facie* case of obviousness established by the Examiner (even if the Examiner had made out a *prima facie* case and, as noted above, the Examiner has failed to establish such a case).

E. The Examiner fails to meet his burden of proof in establishing a *prima facie* case of obviousness under 35 USC §103

As will be seen by the following discussion, the Examiner has not established (1) that all claimed elements and method steps are disclosed in the Cooper/Tobias combination of references, (2) the required explicit "analysis" of his reasoning for picking and choosing elements and then combining them in the manner of

Appellant's independent claims and has not rebutted the clear teaching away from the claimed invention contained in both the Cooper and Tobias references. A detailed discussion of each of these bases for traversing the obviousness rejection follows.

1. The Examiner fails to demonstrate where or how the prior art teaches claimed features

As noted in sections A and B above (incorporated herein by reference), the Examiner is believed to have ignored at least one claimed limitation in each of the independent claims. While the Examiner admits that the Cooper reference fails to disclose the claimed "at least one further circuit," the Examiner's citation of Tobias actually also fails to contain the "at least one further circuit" as required by each of independent claims 1, 6 & 11.

The Examiner is reminded that the Court of Appeals for the Federal Circuit has held that "the PTO has the burden under Section 103 to establish a *prima facie* case of obviousness." *In re Fine*, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). "It can satisfy this burden **only by showing some objective teaching** in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references" (emphasis added). The Examiner has identified no objective teaching in any of the cited prior art references of processor operation at "at least one intermediate data

processing performance level during said change." Thus, the Examiner has clearly failed to meet his burden.

Because the Examiner fails to establish that the claimed "at least one further circuit" is disclosed in at least one of the Cooper/Tobias combination of references, he has failed to meet his burden of establishing a *prima facie* case of obviousness and the rejection of independent claims 1, 6 and 11 (and all claims dependent thereon) is clearly erroneous.

2. The Supreme Court in *KSR* specifically notifies examiners "to facilitate review [of the rationale for combining references], this analysis should be made explicit"

The Examiner, as noted above in section C (incorporated herein by reference), clearly fails to provide any explicit "analysis" or rationale as to why one of ordinary skill in the art would pick and choose elements from the Cooper and Tobias references and then the combine those elements in the manner disclosed only in Appellant's independent claims 1, 6 and 11.

As the Supreme Court stated, "rejections on obviousness grounds cannot be sustained by mere conclusory statements; instead there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *KSR International Co. v. Teleflex, Inc.* 82 USPQ2d 1385, 1396 (SCT 2007) at page 1396.

Accordingly, even if there were some disclosure of an "intermediate data processing performance level during said change" somewhere in one of Cooper and

Tobias, there is no *prima facie* case of obviousness because there is no rationale for picking and choosing the elements/method steps and subsequently combining them in the manner of the independent claims.

3. Any *prima facie* case of obviousness has been rebutted by the teachings of the Cooper and Tobias references

As clearly discussed in section D above (herein incorporated by reference), both the Cooper and Tobias references teach that processing stops during any change in data processing level. Accordingly, each of Cooper and Tobias teaches away from the claimed invention which continues to operate the processor at an intermediate performance level during a change in performance level.

Because both prior art references teach away from this claimed feature of independent claims 1, 6 and 11, Appellant has clearly rebutted any *prima facie* case made by the Examiner.

As seen above in subsections 1-3, there is no basis for an obviousness rejection and thus, any further rejection of independent claims 1, 6 and 11 or claims dependent thereon under 35 USC §103 is respectfully traversed.

VIII. CONCLUSION

Independent apparatus claim 1, method claim 6 and means-plus-function claim 11 all require a specific interrelationship between the "one further circuit" and the "processor" so that there is controlled operation "at said at least one intermediate data processing performance level during said change." This is

missing from both prior art references. Cooper's teaching of a single processor going to a "quiescent" state while changing power levels and Tobias' teaching of a "stop grant state" when changing power levels, not only doesn't teach the claim feature, but is the direct opposite and thus the alleged *prima facie* case falls. The Examiner has failed to provide any "explicit analysis" as to why one would be motivated to combine portions of the two references in the manner of the independent claims and therefore fails to meet his burden of establishing a *prima facie* case of obviousness. The Examiner fails to provide any evidence rebutting the fact conclusion that both references would lead one of ordinary skill in the art away from the claimed invention, thereby rebutting any *prima facie* case of obviousness.

As a result of the above, there is simply no support for the rejection of Appellant's independent claims or claims dependent thereon under 35 USC §103. Thus, and in view of the above, the rejection of claims 1-11 under 35 USC §103 is clearly in error and reversal thereof by this Honorable Board is respectfully requested.

Respectfully submitted,

NIXON & VANDERHYE P.C.

By: _____

Stanley C. Spooner
Reg. No. 27,393

SCS:kmm
Enclosure

IX. CLAIMS APPENDIX

1. Apparatus for processing data, said apparatus comprising:

a processor operable to perform data processing operations, said processor being operable to generate a performance control signal indicative of a desired data processing performance level of said processor; and

at least one further circuit, responsive to said performance control signal, to support said desired data processing performance level of said processor; wherein while responding to a change in performance control signal corresponding to a change from a first desired data processing performance level to a second desired data processing performance level, said at least one further circuit supports data processing of said processor at at least one intermediate data processing performance level and said processor temporarily operates at said at least one intermediate data processing performance level during said change.

2. Apparatus as claimed in claim 1, wherein said one or more further circuits include a voltage controller operable to generate a power signal for said processor at a plurality of different voltage levels.

3. Apparatus as claimed in claim 1, wherein said one or more further circuits include a clock generator operable to generate a clock signal with a selectable clock frequency.

4. Apparatus as claimed in claim 2, wherein, in response to an increase in desired data processing performance level, said clock generator increases clock signal frequency to an intermediate clock signal frequency when said voltage controller is generating a power signal with a voltage level sufficient to support said intermediate clock signal frequency.

5. Apparatus as claimed in claim 1, wherein one or more priority signals serve to trigger said further circuit change to support a predetermined data processing performance level independently of said performance control signal.

6. A method of processing data, said method comprising the steps of:

performing data processing operations with a processor, said processor being operable to generate a performance control signal indicative of a desired data processing performance level of said processor; and

in response to said performance control signal, operating one or more further circuits so as to support said desired data processing performance level of said processor; wherein while responding to a change in performance control

signal corresponding to a change from a first desired data processing performance level to a second desired data processing performance level, said operating step includes supporting data processing of said processor at at least one intermediate data processing performance level and said processor temporarily operates at said at least one intermediate data processing performance level during said change.

7. A method as claimed in claim 6, wherein said one or more further circuits include a voltage controller operable to generate a power signal for said processor at a plurality of different voltage levels.

8. A method as claimed in claim 6, wherein said one or more further circuits include a clock generator operable to generate a clock signal with a selectable clock frequency.

9. A method as claimed in claim 7, wherein, in response to an increase in desired data processing performance level, said clock generator increases clock signal frequency to an intermediate clock signal frequency when said voltage controller is generating a power signal with a voltage level sufficient to support said intermediate clock signal frequency.

10. A method as claimed in claims 6, wherein one or more priority signals serve to trigger said further circuit change to support a predetermined data processing performance level independently of said performance control signal.

11. Apparatus for processing data, said apparatus comprising:

a processor operable to perform data processing operations, said processor being operable to generate a performance control signal indicative of a desired data processing performance level of said processor; and

at least one further circuit, responsive to said performance control signal, for supporting said desired data processing performance level of said processor; wherein while responding to a change in performance control signal corresponding to a change from a first desired data processing performance level to a second desired data processing performance level, said at least one further circuit comprising a means for supporting data processing of said processor at at least one intermediate data processing performance level and said processor temporarily operates at said at least one intermediate data processing performance level during said change.

X. EVIDENCE APPENDIX

None.

XI. RELATED PROCEEDINGS APPENDIX

None.